

U.S. Application No. 09/415,060

Docket No. 0378-0360P

December 31, 2003

Art Unit: 2615

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AMENDMENTS TO THE SPECIFICATION

IN THE SPECIFICATION:

Please replace the paragraph beginning on page 2, line 30 and ending on page 3, line 16 with the following rewritten paragraph.

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cont

On the other hand, the pixel skipping or reduction scheme reduces the number of pixels only in the vertical direction and therefore sacrifices the vertical resolution of a picture. For example, assume that the number of pixels of the image pickup section is four times as great as a VGA (Video Graphics Array) size, and that data are read out of the pixels in accordance with a clock having a frequency of 12 MHz and synchronously displayed on a display of VGA size. Then, it is necessary to reduce the number of pixels to be read to one-fourth. In practice, however, the pixels are reduced to [[one-eight]] one-eighth in the vertical direction field by field in the NTSC or the PAL system so as to implement one-fourth reduction relatively easily. In this case, the pixels are not reduced in the horizontal direction because horizontal reduction is difficult to perform due to the arrangement of the photosensitive devices of the image pickup section. As a result,

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one horizontal period of the image pickup corresponds to two horizontal periods for the display. The picture reduced only in the vertical direction is ill balanced, compared to a picture reduced by half in both of the horizontal and vertical directions.

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Please replace the paragraph beginning on page 6, line 9 and ending on page 6, line 23 with the following rewritten paragraph.

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Cont

Referring to ~~FIGS.~~ FIG. 1 of the drawings, a digital camera including a solid-state image pickup apparatus embodying the present invention is shown and generally designated by the reference numeral 10. As shown, the digital camera 10 includes an image pickup 12, a CDS (Correlation Double Sampling) 14, an ADC (Analog-to-Digital Conversion) 16, a color signal processing 18, a system clock generating section 20, a mode setting 22, a system controller 24 and a clock selector 26 as well as conventional optics not shown. The camera 10 additionally includes an input/output terminal 34 connected to a display 30 and a recording 32 positioned outside of the camera 10. The input/output terminal 34 sends a

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signal output from the color signal processing 18 to the display 30 and/or the recording 32 or receives a signal from the recording 32, as needed.

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Please replace the paragraph beginning on page 6, line 9 and ending on page 6, line 23 with the following rewritten paragraph.

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The multiplexing 46 distributes the colors of the input signals line by line at the period of  $1/\text{clock } f_1$ . As a result, a period of time allocated to, [[e.g,]] e.g. the combination of colors G and R is quadrupled; that is, the signal rate is  $\text{clock } f_2/4$ . To sample each of the colors G and R in such a time zone, the clock  $f_1$  is fed to the ADC as in the illustrative embodiment. This is successful to read the signal at a higher speed than in the still picture mode for the same reason as described in relation the illustrative embodiment. Further, a frame memory which would aggravate the power consumption of the camera 10 is not necessary. In addition, the modification renders the picture well balanced and renders the following processing easy to execute.